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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/617,441	07/14/2000	HIROTAKA KAWATA	106310	5358

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/617,441	KAWATA, HIROTAKA	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,20,21 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,20,21 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 24 is objected to because of the following informalities: In the last line of the claim, "corrects" should be --connects--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3 – 8, 20, 21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Murade (WO 98/16868).

With regard to claim 1, Murade discloses in figures 5 and 6 an electro-optical device. Murade discloses in figures 5 and 6 a substrate (10). Murade discloses in figures 5 and 6 a pixel electrode (14). Murade discloses in figure 5, figure 6, and column 13, lines 49 – 55 (of the English language equivalent to Murade, USPAT 6573955) a scanning line (2) including a main portion and a gate electrode (the main portion being those extending between areas functioning as the gate electrodes). Murade discloses in figures 5 and 6 a data line (3) crossing the scanning line. Murade discloses in figures 5 and 6 a transistor disposed at least in an intersection between the data line and the scanning line, where the data line and the scanning line crass, the transistor

including the gate electrode (portion of 2 in the crossing area) and a semiconductor layer (1, 1a, 1d, 1c, 1e, and 1b). Murade discloses in figures 5 and 6 the gate electrode is disposed outside the intersection where the data line and scanning line cross (at least in the portion directly to the left and right of the data line 3). Murade discloses in figures 5 and 6 the semiconductor layer comprises a source region (1b) that is connected to the pixel electrode through a contact hole (4), a drain region (1a) that is connected to the data line through a second contact hole (5), a channel region (1c) disposed under the gate electrode, and a semiconductor portion (1, figure 5) protruding out of the channel region and not being covered with the gate electrode. Murade discloses in figures 5 and 6 the semiconductor portion protruding out of the channel region and not being covered with the gate electrode only connects directly with the channel region.

With regard to claim 3, Murade discloses in figure 5, figure 6, and column 7, lines 48 – 49 (see USPAT 6573955) the semiconductor region forming the transistor comprises polycrystalline silicon.

With regard to claim 4, Murade discloses in figure 5, figure 6, and column 9, lines 32 – 33 (see USPAT 6573955) the substrate being an insulative substance.

With regard to claim 5, Murade discloses in figure 5, figure 6, and column 9, lines 32 – 33 (see USPAT 6573955) the substrate being a quartz substrate.

With regard to claim 6, Murade discloses in figure 5, figure 6, and column 9, lines 32 – 33 (see USPAT 6573955) the substrate being a glass substrate.

With regard to claim 7, Murade discloses in figures 5 and 6 a second substrate (31) disposed opposing a surface of the first substrate. Murade discloses in figure 5, figure 6, and

column 5, lines 20 – 26 (see USPAT 6573955) liquid crystals sandwiched by the first substrate and the second substrate, and driven by transistor elements formed on the semiconductor layers.

With regard to claim 8, Murade discloses in figure 5, figure 6, and column 6, lines 16 – 21 (see USPAT 6573955) a light source. Murade discloses in figure 5, figure 6, and column 6, lines 16 – 21 (see USPAT 6573955) the electro-optical device according to claim 1 that modulates, in accordance with image information, an incident light emitted by the light source. Murade discloses in figure 5, figure 6, and column 6, lines 16 – 21 (see USPAT 6573955) a projection system that projects a light modulated by the electro-optical device.

With regard to claim 20, Murade discloses in figures 5 and 6 the semiconductor portions protrudes in a direction in which the scanning line extends (the scanning line extending across its width from the top to the bottom of the page in figure 5).

With regard to claim 21, Murade discloses in figures 5 and 6 wherein the gate electrode has two parts protruding out of the semiconductor layer (figure 5, part of 2 between 1c's, and part of 2 directly to the left of leftmost 1c), and the source region being disposed between the two parts (while the source is not directly between the two parts, it should be noted that the gate and the source are on different levels and the source would never be directly between the parts of the gate).

Murade reads on claim 24 as shown in figure 5 wherein a plurality of pixel electrodes, a plurality of scanning lines, a plurality of data lines, and a plurality of transistors are defined.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murade as applied to claim 1 above, and further in view of Watanabe et al. (USPAT 5316960, Watanabe).

Murade does not disclose the semiconductor region forming the transistor comprises monocrystalline silicon. Watanabe teaches in column 4, lines 22 – 26 that monocrystalline silicon is a well known material with which to form a semiconductor region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use monocrystalline silicon of Watanabe as the semiconductor for the transistor of Murade in order to select a layer with desired channel characteristics.

Response to Arguments

6. Applicant's arguments with respect to claims 1 – 8, 20 – 21, and 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703) 308-6236. The examiner can normally be reached on 8:30 AM - 5:30 PM. After February 9th the examiner can be reached at (571)272-1723.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
January 30, 2004

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800